BRAEMAR

APPLICATION NOTE

CM600 — MINI DEK INTERFACE

APPLICATION NOTE
Spec. 0072

INTERFACE INFORMATION

as aplied to
CM600 — MINI DEK

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1.0 MICROPROCESSOR INTERFACING

The most efficient (and simplest) means of interfacing the CM600 to a microprocessor is shown in Figure 1.

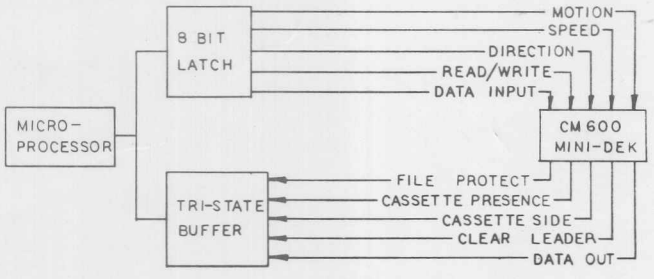

FIGURE 1 MICROPROCESSOR INTERFACE

Such a system has a very low parts count and is easy to implement. All of the encoding and decoding of the data is accomplished in software. (See Braemar Specification 70 for details of phase encoding). Software for some microprocessors is available from the factory, and any additional user-generated software is appreciated by the factory.

1.1 DECODING TECHNIQUES

Experience has shown that a good decoding scheme is extremely important. A variable two thirds cell timer with pulse width averaging (as described in Spec. 70, section 6.4, 6.5) is highly recommended. This system is most frequently implemented with software; however, hardware schemes (sometimes using phase locked loops) may also be used.

Other speed tolerant encoding and decoding schemes used throughout the industry have been applied very successfully and are also recommended, providing that the data is kept within the specified limits. Speed intolerant systems, such as fixed three quarter cell timers (Spec. 70, section 6.1) should not be used. The mean time before service is definably reduced and error rate is increased with speed intolerant decoding schemes.

1.2 INTERFACE LEVELS

The CM600 has some CMOS inputs. As a result a "1" is normally attached with an input voltage slightly above 2.5 volts; however, it is not *guaranteed* until the input reaches 3.5 volts. TTL outputs normally switch high enough to satisfy CMOS inputs; however, inspection of the worst case output specifications of TTL show an incompatibility between TTL outputs and CMOS inputs. The incompatibility between

PMOS outputs and CMOS inputs is even worse, and sometimes TTL and PMOS outputs will not switch high enough for CMOS inputs. If the CM600 is driven from TTL or PMOS, it must be provided with pull-up resistors or some other means of guaranteeing 3.5 volts in the "1" state at the inputs.

The data and clear leader outputs are also CMOS and are capable of sinking at least one TTL load. The other outputs are contact closures to ground and may be handled as desired.

2.0 SEQUENCE OF OPERATION

As mentioned in the manual it is important to avoid operating the machine after it runs out of tape in either direction. Such operation will damage the pucks. Operation in the forward mode after the machine runs out of tape is especially damaging. Listed below is a suggested sequence of operation.

1. Insert tape
2. Rewind (high speed) for 1 second
3. Check for clear leader, observe for 50 ms
4. If clear leader, stop machine immediately
5. If no clear leader, rewind to clear leader and stop machine immediately when clear leader is observed for more than 50 ms. (the 50ms delay assures the operator that he has not stopped on the hole).
6. Place the machine in slow forward and in the write mode (if writing)
7. After observing the hole in tape on the clear leader line start writing or reading data.
8. Write or read the tape until the hole at the end of tape is observed.
9. Stop the machine after completing the last record.

3.0 SUPPLY VOLTAGE

The specification on the CM600 calls for a minimum of 5.0 volts on the supply lines. If the voltage is below 5.0 volts, proper solenoid operation cannot be guaranteed and the machine and tape may be damaged. Care must be taken to assure that at least 5.0 volts is present **at the machine** when it is running in the **rewind** (high speed) mode.

4.0 DATA CAPACITY

The CM600 specifications were drawn up in anticipation of a 100 foot tape. To date such a tape does not exist. At present, the standard tape length is 50 feet, and 80 foot tapes will be available in the near future. Care should be used to interpret the published data capacity specifications based on either a 50 or 80 foot tape.

5.0 RECORD FORMATTING

Convention is to put a preamble consisting of alternating zeros and ones at the beginning of each record. A corresponding postamble is also put at the end of each record (see section 6 of the manual). It is also convention to write a one in the inter-record-gap and to write the least significant bit of the data first. This makes the preamble and postamble a hex AA.

Once the phase encoded data has been written on the tape, the user is faced with the problem (during read) of deciding where the data begins.

If there is extraneous information in the inter-record-gap, the user's software may misinterpret the beginning of the preamble and may end up with shifted data. To eliminate this problem, many users incorporate a "character recognition code" immediately following the preamble and preceding the data. The software is then constructed to look for this character and disregard any information preceding it.

Once the recognition character is received, the software accepts all information following as valid data.

When the transport is switched into the read mode, or powered up, the state of the output data latch is undefined. As a result, the first transition of the preamble may be ignored. The use of a character recognition code also eliminates any problems caused by this situation. If, for some reason, a character recognition code cannot be used, the modification shown on the **attached** schematic diagram in dotted lines may be added to initialize the output to the 1 state each time the machine is started.

6.0 SEARCH AND REWIND

When rewinding the tape, fast speed should always be used. Data will appear at the otuput during fast forward and during rewind; however, it may not be considered valid. The presence (or absence) of this data may be used only to determine record location during fast forward or rewind. For instance, the user may wish to back up 5 records and then read. He simply stops the machine, puts it in rewind and counts five inter-record-gaps (by monitoring the data line) and then stops the machine again and starts reading forward.

7.0 FILE PROTECT

The location of the file protect tab on the mini cassette is not very obvious. File protect on a particular side is accomplished by knocking out the tab as shown in figure 2. To inhibit the write circuit, the user must feed the file protect signal through logic and back to the machine.

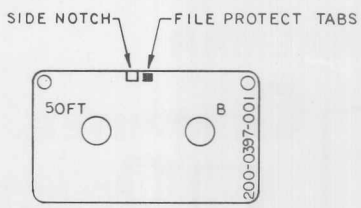

FIGURE 2 DIGITAL MINI CASSETTE

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